6. (Amended) A processor according to Claim 1 wherein:

the instruction is a bit extract instruction that uses an implicitly-derived register specifiers and has a form of:

bitext rsl, rs2, rd,

G3

and per.forms an operation of extracting bits from even-aligned pairs of registers r[rsl] and [rsl+ 1] where the term [rsl+l] designates data contained within the other register following the explicitly-defined register rsl, wherein data in register r[rs2] describes the extracted field of registers r[rsl] and r[rsl + 1] and register r[rd] is a destination register.

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11. (Amended) A processor according to Claim 1 wherein:

the instruction is a double-precision floating point subtraction instruction that uses an implicitly-derived register specifiers and has a form of:

dsub rsl, rs2, rd,

G4

and performs an operation specified by the equation:

(rd, [rd+l]) = (rsl, [rsl+l]) - (rs2, [rs2+1]),

where the terms (rsl, [rsl+l]), (rs2, [rs2+1]), and (rd, [rd+1]) designate double-precision words.

17.(Amended) A processor according to Claim 1 further comprising:

G5

a decoder coupled to the functional unit and configured to generate a first pointer pointing to the explicitly-specified register and a second pointer pointing to the other register.

19.(Amended) A processor according to Claim 1 further comprising:

G6

a pointer coupled to the register file and designating a register in the register file, the pointer including a signal indicative of selection of a the other register, wherein a register read of the explicitly-specified register is accompanied by a register read of the other register when implicit derivation of the explicitly-defined register specifier is selected.

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20. (Twice Amended) A method of operating a processor comprising:
storing information in a register file including a plurality of registers;
executing instructions in a functional unit coupled to the register file and operating upon a plurality of registers in the register file;
G7 explicitly defining a register specifier of a register operated upon during executing of the instruction; and
implicitly deriving a register specifier of at least one other register operated upon during executing of the instruction based on the explicitly defined register specifier.

21. (Amended) A method according to Claim 20 further comprising:
G8 decoding an instruction; and
deriving, during decoding of the instruction, a register specifier based on the explicitly-specified register specifier of the instruction.

24. (New) A method according to Claim 20 further comprising:
G9 implicitly deriving the register specifier for the other register by adding one to the explicitly-defined register specifier.

REMARKS

Claims 1, 3, 6, 11, 19, 20 and 21 are amended. New claim 24 has been added.

No new matter has been added. Examination on the merits is respectfully requested.

If the Examiner has any questions, Applicants respectfully request that the Examiner contact the undersigned at the telephone number indicated below.